Silicon Micromachined RF MEMS Resonators

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ABSTRACT — **A new resonator concept based on three dimensional (3D) high resistivity silicon substrate filled cavity resonators is investigated. Fabrication is done using micromachining technologies. Two types of resonators are investigated, an "open-end" patch resonator and a "short circuit via" resonator. Both types show good agreement in simulated and measured resonance frequencies (within 2%). However, measured quality factors (50-70) are still lower than the simulated values and theoretical expectations.**

I. Introduction

With the increasing demand of broadband and mobile wireless communication systems, the need for high-performance, low-cost, low-power and small-size microwave circuits becomes more pronounced. One of the most important components in such a wireless system is the bandpass filter that is used both in the receiver and the transmitter for keeping unwanted signals away from other parts of the system. These bandpass filters are also key elements for future direct digital RF receivers. In order to achieve the superior performance required by these applications, the filters need to be designed with high-quality factor resonators.

Such resonators are typically built using waveguide components. In the lower microwave frequency range, however, waveguides are large, very difficult to integrate with other planar circuits and costly to manufacture. During the last years, therefore, several groups have developed silicon micromachined cavity and membrane resonators that can provide superior quality factors at microwave frequencies [1-5]. These resonators are planar, monolithic and have a low production cost potential.

In this paper a new resonator concept is investigated, which uses the semiconductor substrate as a cavity. It is based on a three dimensional (3D) dielectric filled resonator and employs micromachining technologies for fabrication. Electromagnetic simulations and experimental realizations are given.

II. Resonator Concept

The basic idea of the resonator concept is the well-known three-dimensional (3D) cavity resonator. The proposed 3D resonators are fabricated directly in the substrate wafer: backside metallization forms the bottom of the resonator. Its sidewalls are realized by via-hole fences. The top cover is formed by the metallized and patterned front side of the substrate (see Figs. 1 and 2). With this concept, fabrication is possible on a single wafer. Since only via holes have to be micromachined, all metallization lines and coupling structures can be fabricated on planar, solid surfaces as in common microelectronic processing. Due to the high dielectric constant ε_r of the silicon substrate, a size reduction is achieved in comparison to air-filled cavity resonators.

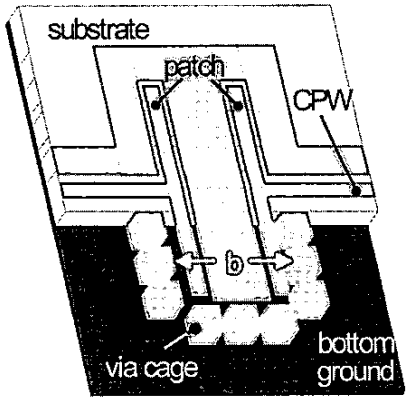

Fig. 1. The patch resonator (substrate in the lower half blanked to show the vias, not drawn: a denotes cavity dimension in vertical direction).

For the well-known 3-dimensional cavity resonator the lowest resonance frequency is determined by the two largest dimensions *a (length)*and *b(width)* of the cavity as

$$f = \frac{c_0 * \sqrt{\frac{1}{a^2} + \frac{1}{b^2}}}{2 * \sqrt{e_r}} \qquad (1)$$

Proceeding from this ideally closed 3-dimensional cavity resonator several resonators with via cages were developed, varying the coupling structures for exciting and probing the inner resonant fields. In this paper, we present

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two types of the various MEMS-technology based structures.

Basically, these two structures differ with regard to excitation. One is an "open-end" patch resonator (Fig. 1), the other a "short-circuited" via resonator (Fig. 2). Both are fed by CPWs. In the patch resonator, the electric field from the patch to the ground planes and vias couples into the resonator, in the short-via resonator, the magnetic field of the current through the via excites the field in the resonator. The vias used have a diameter of 250 µm and are spaced in a distance of about 100..150 µm. To first order, this dense chain of metallized vias acts like an entirely closed sidewall.

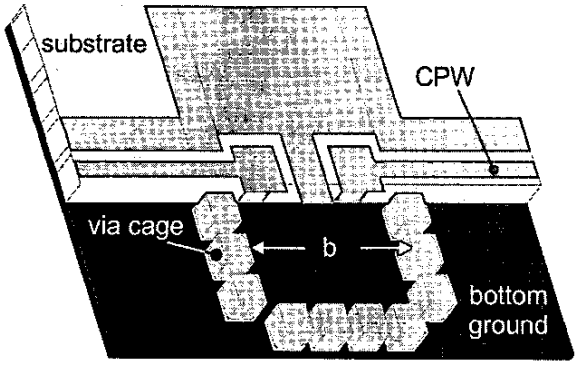

Fig. 2. The short-via resonator (substrate in the lower half blanked to show the vias)

III. Fabrication Process

The fabrication process of the 3D resonators (Fig 3) is performed on 4 inch high-resistivity silicon ($\rho > 5000\ \Omega$cm) wafers. Before processing, the wafers are polished on both sides to a thickness of 250 µm. This thickness is chosen to achieve a proper via-hole fabrication. After a cleaning process, the wafers are thermally oxidized to an oxide thickness of 50 nm. Next the oxide was removed on the places where the via holes have to contact the resonator metallization top layer (using mask level 1).

Then the metallization layers (20 nm Ti, 2200 nm Au) are defined using a lift-off process and mask level 2. This process yields very smooth surfaces of the gold metallization and very steep edges of the metallization layer. With a back side to front side alignment process the via hole are defined in thick photoresist (using mask level 3). The via holes are etched with an anisotropic deep silicon etch process as described in [6]. Vertical sidewalls are achieved with this dry etch process (see Fig. 4). After removal of the residual photoresist in an oxygen plasma the via holes and the backside of the wafer is metallized by sputtering 100 nm TiW as adhesion and interdiffusion layer and 2000 nm Au as metallization layer. This completes the fabrication process of the 3D micromachined resonators.

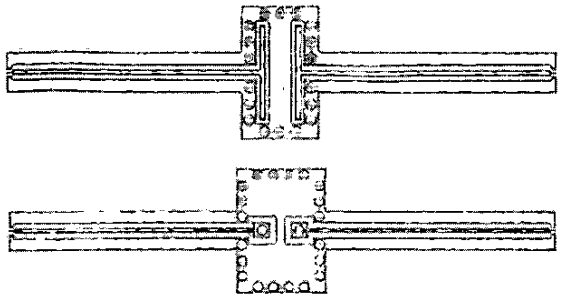

Fig 3.: Layout of the patch and via coupled resonators

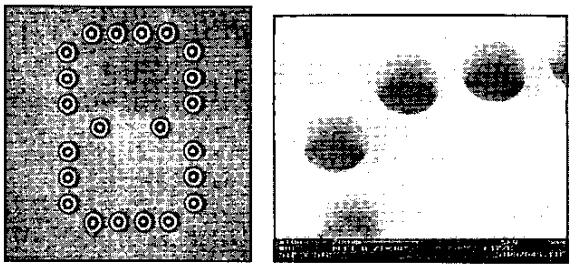

Fig 4.: Photo and SEM of metallized via hole chain, which forms the sidewall of the 3D resonator

IV. Electromagnetic Simulation And Measurement Results

The calculations were carried out using the finite-difference method in frequency domain, taking into account both the CPW- and the parasitic parallel-plate-(PPL)-mode, which can propagate also due to the backside metallization.

The characteristic dimensions of the patch resonator presented are $a = 2300$ µm, $b = 1100$ µm, the thickness of the silicon wafer is 250 µm and the dielectric constant of the high-resistivity Si is $\varepsilon_r = 11.7$ assuming a $\kappa = 0.01$S/m (corresponding to a substrate resistivity of 10 kΩcm).

The short-via resonator is of size $a = 2300$ µm, $b = 1500$ µm. The other dimensions and properties are the same as for the patch resonator.

Tab. 1 provides the theoretical resonance frequencies assuming half-wavelength resonances with regard to a and b as well as the first cavity resonance according to eqn. 1. They can serve as a first-order approximation for the resonators under consideration.

Table 1 : Theoretical values of resonance frequencies.

$\lambda/2$ across dimension	f_{res} / GHz of the patch resonator	f_{res} / GHz of the short via resonator
a	19.1	19.1
b	39.9	29.2
a and *b*	44.2	34.9

For the patch and the short-via resonator the simulated and measured S-parameters are shown in Fig. 5 and 6. One finds good agreement with a frequency shift less than 0.5 GHz.

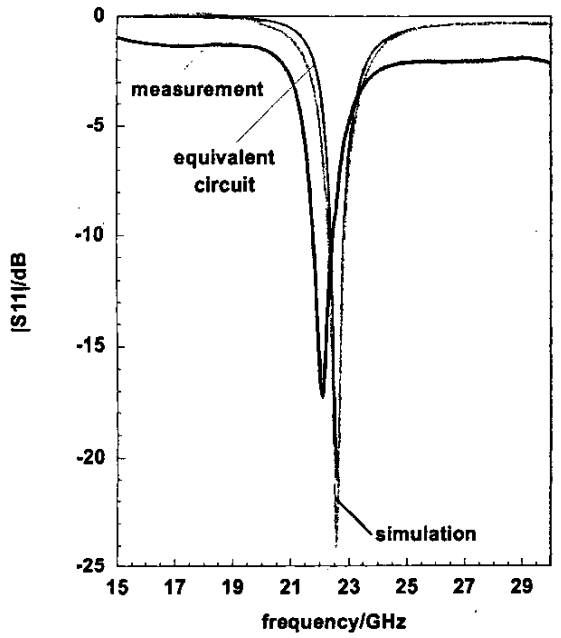

Fig. 5. S_{11} parameter of the patch resonator for
-finite difference (FD) simulation
- equivalent circuit extracted from FD data
-measurements.

In both cases, the shift in resonance frequency between simulation and measurement is attributed to small geometrical deviations between simulated and processed structures and to fabrication tolerances.

Due to the fact, that in S-parameters the ports are matched by 50 Ω lines, the resonance in the S parameters is different from that of the unloaded system. Therefore, the S parameter are converted into Z parameters. For the unloaded resonator, the behaviour of abs(Z_{12}) of the equivalent Z matrix is of interest, which is plotted in Fig. 7. From this curve, we find resonant frequencies of f_{res}= 22.27 GHz (simulation) and f_{res}= 22.00 GHz (measurements) for the patch resonator. For the short-via type, one has f_{res}= 32.0 (32.5) GHz.

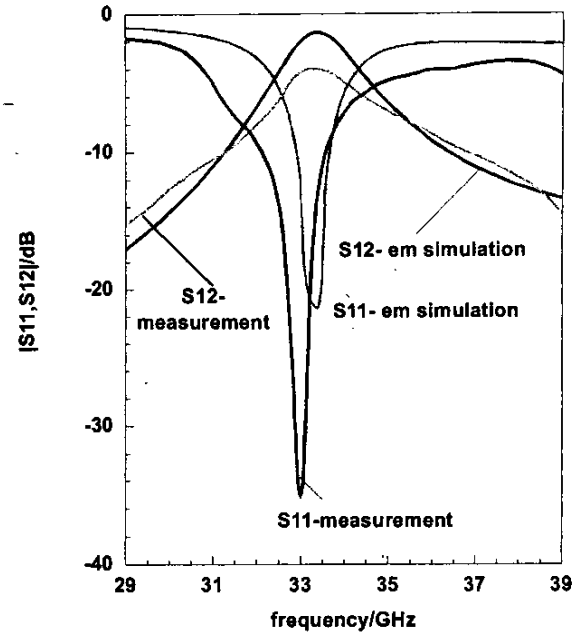

Fig. 6. S-parameters of the short via resonator for em simulation (finite-differences) and measurement.

Comparing the results to the simple approximations in Tab. 1, one observes that the patch resonance is related to the lateral dimension a, whereas for the short via type treated here the longitudinal dimension b is important. Obviously, the nonideal sidewalls (with a gap below the CPWs) as well as the signal short vias and the surface metallization shapes are the reason for the frequency shift compared to the values in Tab. 1.

The quality factor is determined from the well-known bandwidth/center frequency definition as

$$Q = \frac{fres}{f_{\frac{1}{\sqrt{2}}} - f_{\frac{1}{\sqrt{2}}}} \qquad (2)$$

achieving a value of about 70 (simulated value is 120 including losses) for the patch resonator and about 50 for the short-via resonator. One should note that the measured values include the effect of a 5 mm long CPW on either side of the resonators. Both designs form a first step to

determine the performance of these resonators and to develop optimized geometries.

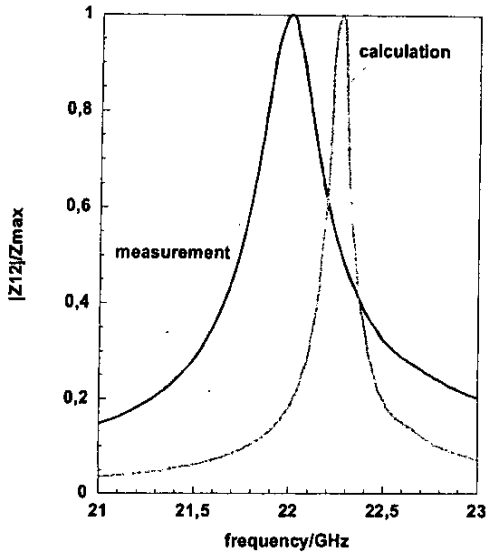

Fig. 7. Z_{12} parameter of the patch resonator (comparison between simulation and measurements).

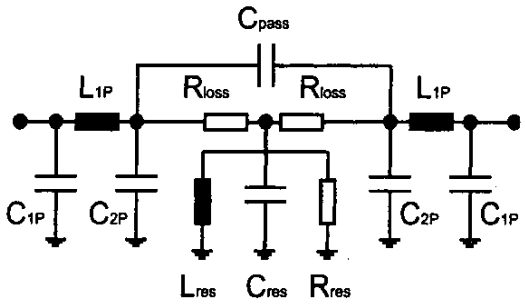

Fig. 8. Equivalent circuit describing the patch resonator.

As can be seen from Fig. 5, the equivalent circuit in Fig. 8 describes the resonator over a wide frequency range around the center frequency. From this circuit, we can draw some important conclusions. E.g., elements which disturb the pure resonator can be identified, such as the capacitance C_{pass}, which short-circuits a part of the coupling energy, or the C_{1P}-L_{1P}-C_{2P}-combinations at the ports of the structure, which describe the properties of the current and voltage path on the patch. More detailed calculations reveal that the capacitance C_{pass} increases with decreasing distance between the patches or between the signal short-vias. Further investigations are in progress in order to reduce such effects by avoiding parasitic coupling.

V. Conclusions

Silicon micromachined 3D MEMS resonators for microwave frequencies have been realized with a relatively simple fabrication process in K-band. Two types of resonators are investigated, an "open-end" patch resonator and a "short circuit via" resonator. Both types show good agreement in simulated and measured resonance frequencies (within 2%).

However, the measured quality factor (50-70) differs from the simulated value (120) and from the theoretically expected values (up to 450). It is expected that this gap can be closed by using optimized resonator geometries. Insulating substrates and higher conductive metallization layers (Cu, Ag) are further options to achieve higher Q values.

Further theoretical investigations with air-filled patch-type resonators show far better quality factors of more than 360 due to larger volume and lower dielectric losses.

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